



ROHDE & SCHWARZ

USER MANUAL



Function Generator

TS-PFG



User Manual

for ROHDE & SCHWARZ Function Generator TS-PFG

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If you have any technical queries about this Rohde & Schwarz equipment, our Hotline at the Support Center of Rohde & Schwarz Sales-GmbH will be glad to help.

Our team will discuss your queries and look for solutions to your problems.

The Hotline is open Mondays to Fridays from 08.00 to 17.00 hrs.

For queries outside office hours, you can leave a message or send a note via fax or email. We will then get back to you as soon as possible.



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1 Usage

1.1 General

The ROHDE & SCHWARZ Function Generator Module TS-PFG can be used wherever single or multiple channel analog output signals have to be simulated.

The floating output of the signals prevents any interference on the unit under test (UUT), thereby ensuring that the application can be simulated under conditions that are very close to actual.

The high dynamic range of the output voltage and the high sample rate achieve a very fine resolution of the output signals. The module can generate standard signal forms such as sine, triangular and square as well as arbitrary forms. These can be output continuously or in pulsed mode.

Commercially available waveform editors can be used for defining the signal curves (e.g. VisualBench by National Instruments). Comprehensive trigger options with local trigger and market signals or the PXI trigger bus facilitate synchronization with other R&S measurement, stimulus or switching modules or PXI modules of other manufacturers.

A LabWindows IVI driver is provided on the card for the general functions. Other hardware functions are controlled using specific extensions of the driver. As is typical for a LabWindows driver, Function Panels and Online Help are available.

The TS-PFG module is inserted in the front of the CompactTSVP chassis. It uses the cPCI/PXI standard. The front connector ends flush with the front panel of the CompactTSVP chassis and is used for contacting UUTs or measurement sensors. At the back, the TS-PFG module is connected to the cPCI control bus and the PXI trigger bus. Instead of using the front connector, analog measurement signals can be captured via the CompactTSVP's analog measuring bus.



The TS-PPFG module can only be used in the CompactTSVP (TSVP = Test System Versatile Platform).

1.2 Characteristics

The TS-PFG Function Generator Module features the following characteristics:

Characteristics TS-PFG
2-channel arbitrary function generator (both channels can be operated as independent generators)
Floating signal generation (max. 125V working voltage)
Resolution (16 bit)
High sample rate per channel (max. 25 MS/s)
High output voltage ranges ($\pm 1V \dots \pm 20 V$), up to 40 Vpp (channels can be cascaded)
High output current (max. ± 250 mA/per channel)
1 MSamples memory depth per channel
Waveform linking and looping
Synchronizing with the PXI trigger bus
Channels can be optionally switched to 8 analog buses/outputs
Self-test capability in conjunction with the TS-PSAM module
LabWindows IVI driver
Used in the <i>CompactTSVP</i>

Table 1-1 Characteristics TS-PFG

1.2.1 Applications

The following applications can be run with the TS-PFG function generator:

- Generating symmetrical sine, square, sawtooth and triangular functions
- Generating random linkable curve forms
- Sensor simulation (floating stimulation)
- Simulating arbitrary signals
- Stimulating low-frequency digital signals with variable level
- Programmable clock-pulse generators
- Generating UUT supply voltages



Should the application require additional stimulus channels, this can be achieved by adding further TS-PFG function generator modules and synchronizing them with the PXI Triggerbus.

The analog bus and an R&S switching module such as the TS-PMB can be used to multiplex the output signals over a very high number of UUT pins.

Complex test operations can be performed by the digital marker signal which is output sample-synchronously with the analog signal. Using a switchable connection of the two output channels, the output voltage range (level +6 dB) can be doubled and/or DC signals generated with modulated-up AC signals.

The extremely compact design with primary matrix and signal conditioning occupies just a single Compact PCI/PXI slot width, making it possible to create space-saving yet very powerful measurement and stimulus systems.

A self-test of the TS-PFG function generator can be run in conjunction with the TS-PSAM module. Diagnostic LEDs in the front panel indicate the module's current status.



2 View

Figure 2-1 shows the TS-PFG Function Test Module without the associated TS-PDC rear I/O module. The TS-PDC rear I/O module is shown in Figure 2-2.



Figure 2-1 View of the TS-PFG module



Figure 2-2 View of the TS-PDC rear I/O module.

3 Block Diagrams

This section provides a function chart of the TS-PFG module as well as a detailed circuit diagram.

Figure 3-1 shows the function chart of the TS-PFG module.

Figure 3-2 shows a detailed block diagram of the TS-PFG module.

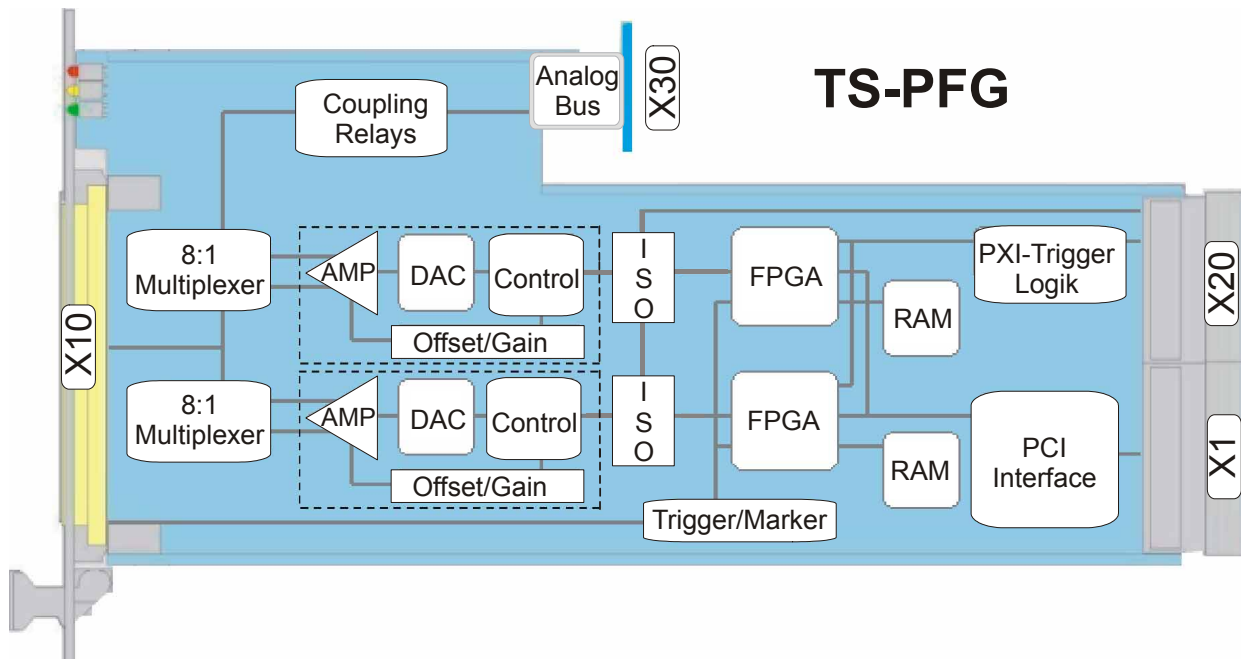


Figure 3-1 Function chart of the TS-PFG module

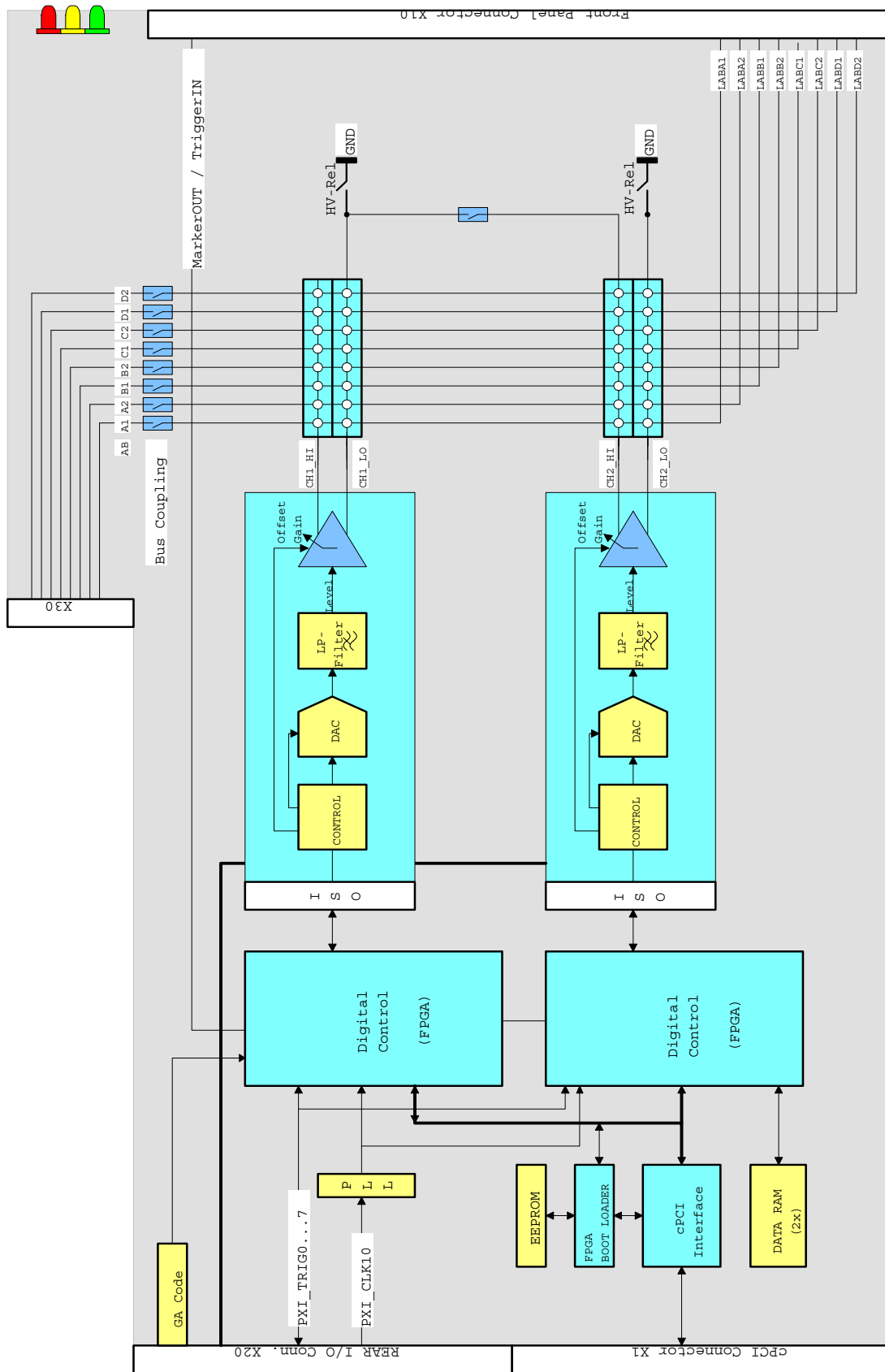


Figure 3-2 Detailed block diagram of the TS-PFG module

4 Layout

4.1 Mechanical construction of the TS-PFG

The TS-PFG module is designed as a **long cPCI plug-in module** for mounting in the front of the CompactTSVP. The board height of the module is 3 HU (134 mm). The front panel is provided with a locating pin to ensure that it is correctly inserted into the Compact TSVP. The module is secured in place with the two retaining screws on the front panel. Front connector X10 is used for connecting the UUTs. Connector X30 connects the TS-PFG module to the analog bus backplane in the CompactTSVP. X20/X1 connectors connect the TS-PFG module to the cPCI backplane/PXI control backplane.

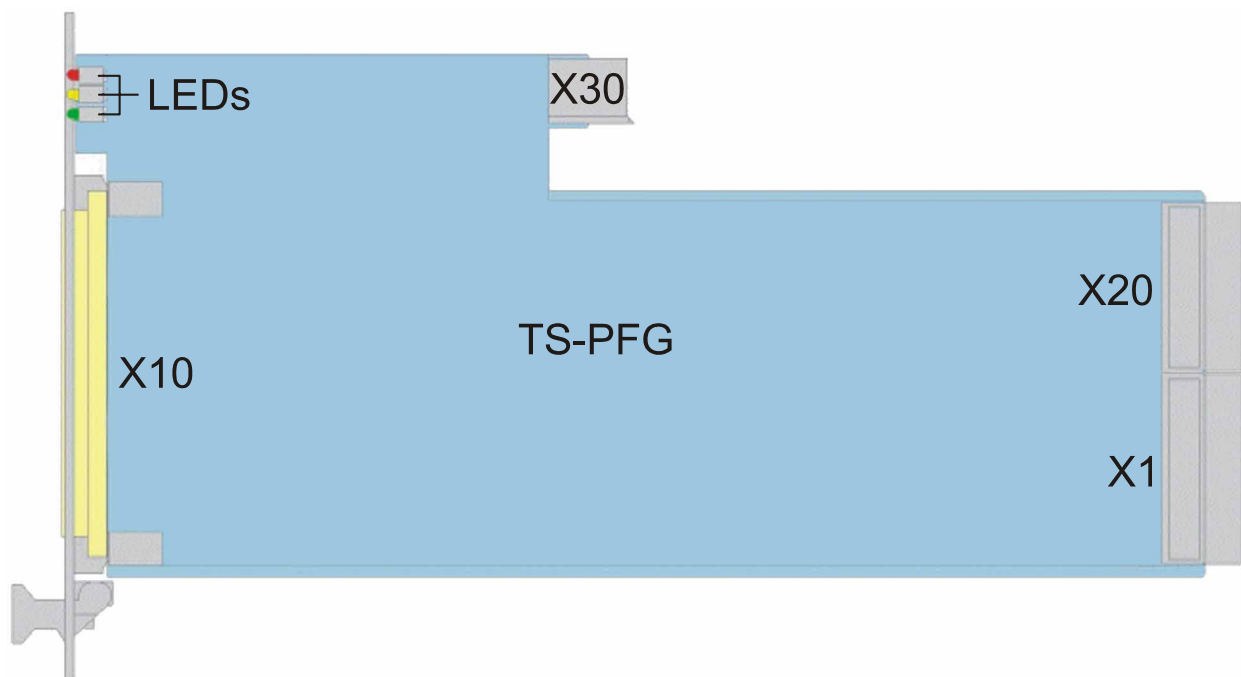


Figure 4-1 Layout of the connectors on the TS-PFG module

Symbol	Use
X1	cPCI Bus
X10	UUT
X20	Extension (PXI), Rear I/O
X30	Analog Bus

Table 4-1 Connectors of the TS-PFG module

4.2 Display Elements on the TS-PFG Module

Three light-emitting diodes (LEDs) on the front of the TS-PFG module indicate its current status. These LEDs have the following meanings:

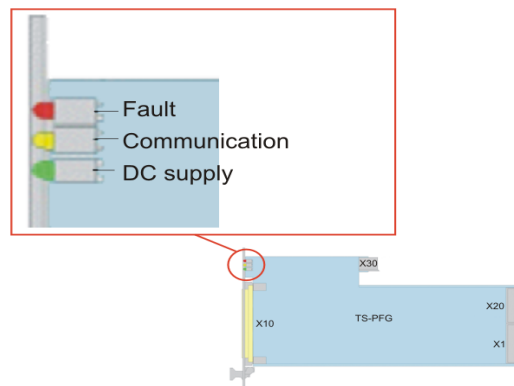


Figure 4-2 Layout of the LEDs on the TS-PFG module

LED	Description
red	Fault (ERR): Lights up when a fault is detected on the TS-PFG module during the power-on test after the supply voltage is switched on. This indicates the presence of a hardware problem on the module. (see also Section 8 “Self-Test”)
yellow	Communication (COM): Lights up when data is exchanged across the interface.
green	Supply voltage OK (PWR): Lights up when all the necessary supply voltages are present.

Table 4-2 Display elements on the TS-PFG module

4.3 Mechanical construction of the TS-PDC

On this topic, see also Figure 4-3

The TS-PDC module is a **rear I/O module** for mounting in the back of the CompactTSVP. The board height of the module is 3 HU (134 mm). The module is secured in place with the two retaining screws on the front panel. Connector X20 connects the TS-PDC module to the extension backplane in the CompactTSVP. The TS-PDC module must always use the corresponding rear I/O slot for the main module (e.g. TS-PSAM module).



WARNING!

The TS-PDC module must always be inserted in the corresponding rear I/O slot (same slot code) of the TS-PFG module. If modules are inserted incorrectly (e.g. cPCI/PXI standard modules in the front), both modules may be damaged irreparably.

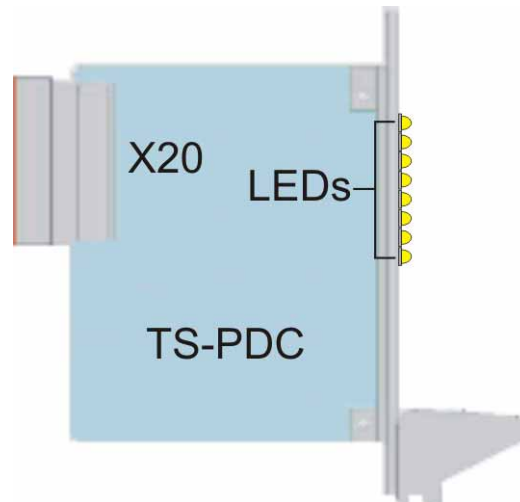


Figure 4-3 Arrangement of the connector and LEDs on the TS-PDC module

Symbol	Use
X20	Extension (Rear I/O)

Table 4-3 Connector for the TS-PDC module

4.4 Display elements of the TS-PDC module

On this topic, see also Figure 4-4

Eight light-emitting diodes (LEDs) are located on the front of the TS-PDC module to show the current status of the generated supply voltages. The individual LEDs have the following meanings:

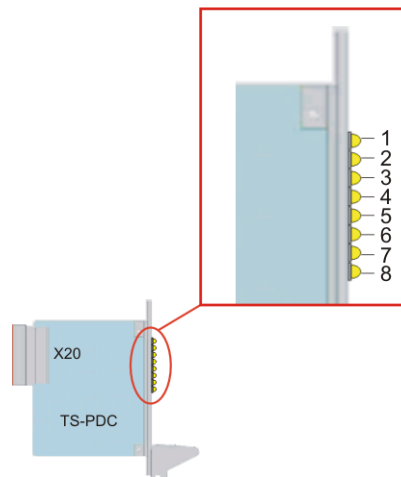


Figure 4-4 Arrangement of LEDs on the TS-PDC module

LED	Description
1, lights up	+15 VDC (CH1), present
2, lights up	+5 VDC (CH1), present
3, lights up	+3.3 VDC (CH1), present
4, lights up	-15 VDC (CH1), present
5, lights up	+15 VDC (CH2), present
6, lights up	+5 VDC (CH2), present
7, lights up	+3.3 VDC (CH2), present
8, lights up	-15 VDC (CH2), present

Table 4-4 Display elements on the TS-PDC module

5 Function Description

5.1 Function Description of the TS-PFG Module

5.1.1 Analog Hardware of the Module

2 independent data paths each with its own voltage potential are used to output the analog stimulus values. All output paths are identical in structure.

Each path has a fast D/A converter to which three "low-pass filters" and a differential power amplifier with adjustable level range are connected on the load side.

The reference bus control unit (FPGA) transmits the digital data over an insulated parallel port at the maximum possible data rate. The FPGA updates the D/A converter for each individual channel as a function of the selected sample rate.

All of the necessary digital control signals (system clock, update signal, amplifier setting) are generated by the FPGA and also transmitted to the analog section by insulation transmitters.

The module derives the voltage supply to the analog front end from a rear I/O module (TS-PDC) with DC/DC converter.

The analog signals are taken out via isolating relays at the module's front connector (X10) and to the analog measurement bus of the CompactTSVP. Fixed current limiting is provided. Higher output voltages can be generated by a direct coupling of the isolated individual channels.

5.1.2 Synchronizing

Triggers can be both received and generated to allow synchronizing with other devices, especially with analyzer modules or digital measuring modules.

The trigger signals of the PXI trigger bus and two trigger input signals to ground with programmable threshold are provided for this purpose.

A phase-locked marker signal can also be generated with an unused bit of the digital output values.



5.1.3 Special Features for Standard Curve Shapes

Standard waveforms (sine, rectangle, triangle, saw tooth) can be generated with the TS-PFG module to match the frequency very precisely. In the case of waveforms with steep edges (rectangle, saw tooth), however, shifts may occur in the edges that are not visible with other curve shapes. The shift (jitter) matches a sampling interval, i.e. 40 ns for signal frequencies above 1 Hz.

To generate signals free of jitter, the signal frequency must be selected so that the duration of the period or (in the case of a rectangle) the pulse width is an integer multiple of 40 ns, or the signal must be programmed as an arbitrary waveforms.

5.2 Function Description of the TS-PDC Module

On this topic, see also Figure 5-1

The DC/DC converter is configured as a primary reference DC/DC converter. The input voltage (5 VDC) is transferred to two secondary potentials and rectified to the nominal voltage by line controllers. The status of the output voltage is displayed in each case by an LED.

The following DC voltages are generated:

- +15 VDC, 0.5A (2x)
- -15 VDC, 0.5A (2x)
- +5 VDC, 0.5A (2x)
- +3.3 VDC, 0.25A (2x)

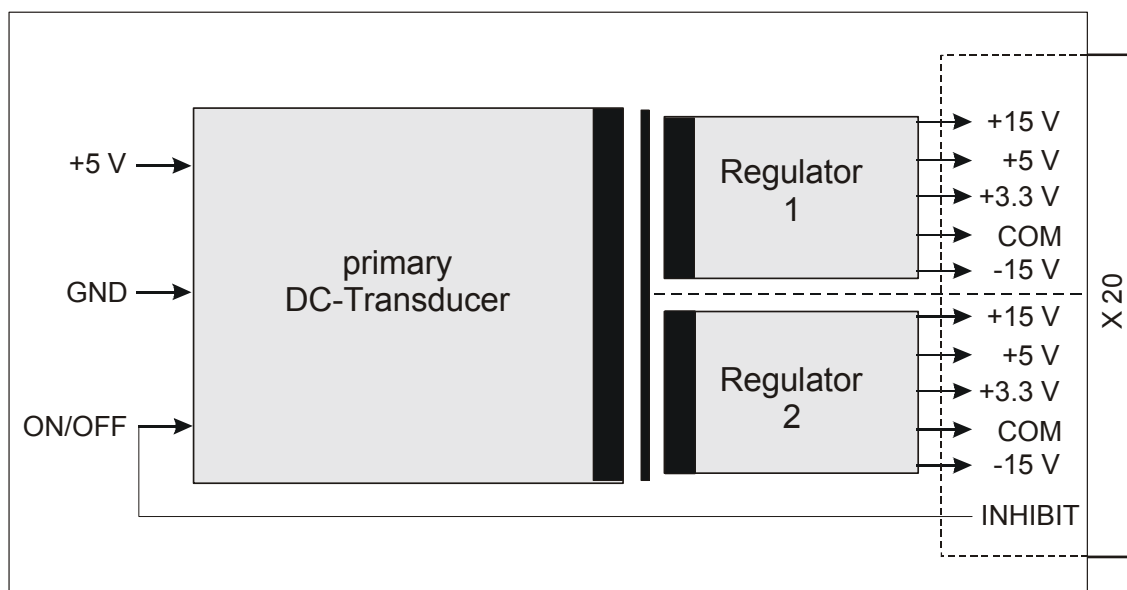


Figure 5-1 Block Diagram of TS-PDC



6 Commissioning

6.1 Installing the TS-PFG Module

To install the plug-in module, proceed as follows:

- Power down and switch off the CompactTSVP
- Select a suitable front slot (slots 5-15 possible, preferably slot 5)
- Remove the corresponding front panel portion from the TSVP chassis by loosening the two screws

**WARNING!**

Check the backplane connectors for bent pins! Any bent pins must be straightened!

Failure to do this may permanently damage the backplane!

- Apply moderate pressure to insert the plug-in module (use locating pin to attach)

**WARNING!**

To insert the plug-in module, use both hands to guide carefully into the backplane connectors.

- The module is correctly located when a distinct 'stop' can be felt.
- Tighten the two retaining screws on the front panel of the module.



The TS-PFG module is automatically detected by the CompactTSVP.



6.2 Installing the TS-PDC Module

To install the plug-in module, proceed as follows:

- The TS-PFG module must have been installed beforehand
- Select the corresponding rear I/O slot for the TS-PFG module
- Remove the corresponding rear panel portion from the CompactTSVP chassis by loosening the two screws



WARNING!

Check the backplane connectors for bent pins! Any bent pins must be straightened!

Failure to do this may permanently damage the backplane!

- Push in the plug-in module using moderate pressure



WARNING!

To insert the plug-in module, use both hands to guide carefully into the backplane connectors.

- The module is correctly located when a distinct 'stop' can be felt.
- Tighten the two retaining screws on the front panel of the module.

7 Software

7.1 Driver Software

A LabWindows IVI driver is provided on the card for the PFG functions. All other hardware functions are controlled using specific extensions of the driver. The driver is part of the ROHDE & SCHWARZ GTSL software. All the functions of the driver are described fully in the on-line help and in the LabWindows CVI Function Panels.

The following software modules are installed during driver installation:

Module	Path	Remarks
rspfg.dll	<GTSL Verzeichnis>\Bin	Driver
rspfg.hlp	<GTSL Verzeichnis>\Bin	Help file
rspfg.fp	<GTSL Verzeichnis>\Bin	LabWindows CVI Function Panel File, Function Panels for CVI Development Environment
rspfg.sub	<GTSL Verzeichnis>\Bin	LabWindows CVI Attribute File. This file is needed by some „Function Panels“.
rspfg.lib	<GTSL Verzeichnis>\Bin	Import Library
rspfg.h	<GTSL Verzeichnis>\Include	Header File for the Driver

Table 7-1 Driver InstallationTS-PFG



NOTE:

The IVI and VISA libraries produced by National Instruments are needed to run the driver.

7.2 Soft Panel

(see Figure 7-1)

A soft panel TS-PFG is provided for the module. The soft panel is based on the LabWindows CVI driver and enables the module to be operated interactively. Special test functions can be activated with a protected menu.

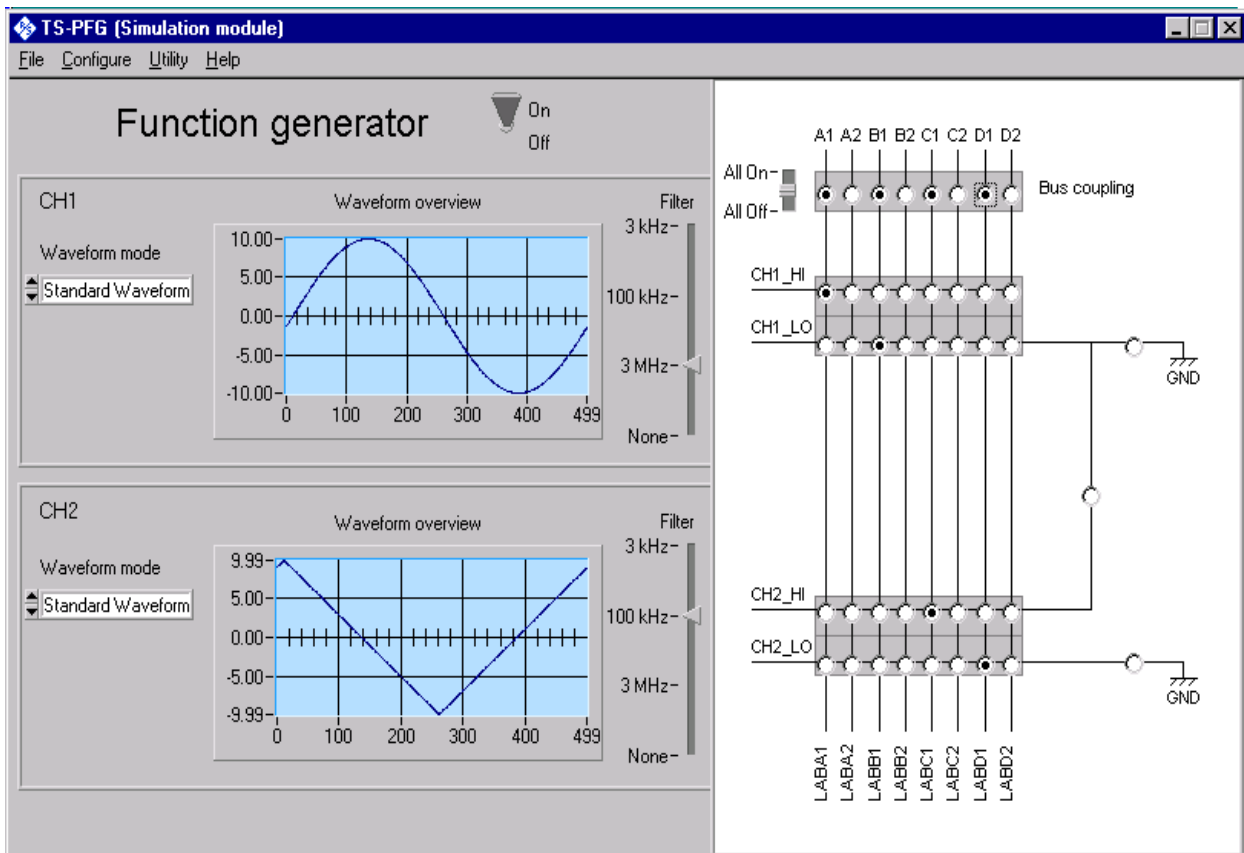


Figure 7-1 Soft Panel TS-PFG

7.3 TS-PFG Programming Example

```
/*
    Generating different output signals
    with and without trigger conditions

    The different examples just show the order of function
    calls used to output a special signal

    The coding rules of a GTSL software like
    allocating and locking the resource, or error handling
    are not considered in this example.
    It's just to show the function calls.
*/

/*
    rspfg ivi-driver header file
*/

#include "rspfg.h"

static ViSession    s_VI;
static ViStatus     s_status;

main()
{
    /*
        The resource descriptor must be adapted to the system:
        Init the rspfg driver.
        After the fuction call the module will generate a dc voltage output
        signal of 0 volts.
    */

    s_status = rspfg_InitWithOptions ( "PXI2::13::0::INSTR", VI_TRUE,
    VI_TRUE, "", &s_VI);

    /*
        Stop generation of output signal.
    */

    s_status = rspfg_AbortGeneration (s_VI);

    /*
        Connect channel 1 to front connector X10.
    */

    s_status = rspfg_Connect (s_VI, "CH1_Lo", "ABa2");

    s_status = rspfg_Connect (s_VI, "CH1_Hi", "ABa1");
}
```



```
/*
  Connect channel 2 to front connector X10.
*/

s_status = rspfg_Connect (s_VI, "CH2_Lo", "ABb2");
s_status = rspfg_Connect (s_VI, "CH2_Hi", "ABb1");

/*
  Wait until switching relays are settled.
*/

s_status = rspfg_WaitForDebounce (s_VI, 1000);

/*
  Configure continuous generation of the output signal.
*/

s_status = rspfg_ConfigureOperationMode (s_VI, "CH1",
RSPFG_VAL_OPERATE_CONTINUOUS);

/*
  Configure continuous generation of the output signal.
*/

s_status = rspfg_ConfigureOperationMode (s_VI, "CH2",
RSPFG_VAL_OPERATE_CONTINUOUS);

/*
  Configure standard function output.
*/

s_status = rspfg_ConfigureOutputMode (s_VI, RSPFG_VAL_OUTPUT_FUNC);

/*
  Configure sine wave output with 1.0 volts amplitude peak to peak on
  channel 1 and channel 2 with
  frequency: 1000 Hz,
  phase: 0 Hz,
  dc offset voltage: 0.0 volt.
*/

s_status = rspfg_ConfigureStandardWaveform (s_VI, "CH1",
                                             RSPFG_VAL_WFM_SINE, 1.0,
                                             0.00, 1000, 0.00);

s_status = rspfg_ConfigureStandardWaveform (s_VI, "CH2",
                                             RSPFG_VAL_WFM_SINE, 1.0,
                                             0.00, 1000, 0.00);
```



```
/*
   Select the output filter 3 kHz to get best signal quality
   for the 1 kHz frequency.
*/

s_status = rspfg_ConfigureFilter (s_VI, "CH1", VI_TRUE, 3.0e3
/*3kHz*/);

s_status = rspfg_ConfigureFilter (s_VI, "CH2", VI_TRUE, 3.0e3
/*3kHz*/);

/*
   Enable signal generator output.
*/

s_status = rspfg_ConfigureOutputEnabled (s_VI, "CH1", VI_TRUE);
s_status = rspfg_ConfigureOutputEnabled (s_VI, "CH2", VI_TRUE);

/*
   Initiate generating signal generator output.
*/

s_status = rspfg_InitiateGeneration (s_VI);

/*
   Stop generation of output signal.
*/

s_status = rspfg_AbortGeneration (s_VI);

/*
   Select the output filter 100 kHz to get best signal quality
   for the 5 kHz frequency.
*/

s_status = rspfg_ConfigureFilter (s_VI, "CH1", VI_TRUE, 1.0e5
/*100kHz*/);

/*
   Configure sine wave output with 1.0 volts amplitude peak to peak,
   with
   frequency: 5000 Hz,
   phase: 0 Hz,
   dc offset voltage: 0.0 volt.
*/

s_status = rspfg_ConfigureStandardWaveform (s_VI, "CH1",
                                             RSPFG_VAL_WFM_SINE, 1.0,
                                             0.00, 5000, 0.00);
```



```
/*
  Initiate generating signal generator output.
*/

s_status = rspfg_InitiateGeneration (s_VI);

/*
  Stop generation of output signal.
*/

s_status = rspfg_AbortGeneration (s_VI);

/*
  Configure number of bursts.
*/

s_status = rspfg_ConfigureBurstCount (s_VI, "CH1", 2);

/*
  Configure burst generation of the output signal.
*/

s_status = rspfg_ConfigureOperationMode (s_VI, "CH1",
RSPFG_VAL_OPERATE_BURST);

/*
  Configure sine wave output with 1.0 volts amplitude peak to peak,
  with
  frequency: 1000 Hz,
  phase: 0 Hz,
  dc offset voltage: 0.0 volt.
*/

s_status = rspfg_ConfigureStandardWaveform (s_VI, "CH1",
                                             RSPFG_VAL_WFM_SINE, 1.0,
                                             0.00, 1000, 0.00);

/*
  Initiate generating signal generator output.
*/

s_status = rspfg_InitiateGeneration (s_VI);

/*
  Start generating signal generator output.
*/

s_status = rspfg_SendChannelSoftwareTrigger (s_VI, "CH1");
```




```
/*
  Stop generation of output signal.
*/

s_status = rspfg_AbortGeneration (s_VI);

/*
  Configure sine wave output with 1.0 volts amplitude peak to peak,
  with
  frequency: 5000 Hz,
  phase: 0 Hz,
  dc offset voltage: 0.0 volt.
*/

s_status = rspfg_ConfigureStandardWaveform (s_VI, "CH1",
                                             RSPFG_VAL_WFM_SINE, 1.0,
                                             0.00, 10000, 0.00);

/*
  Initiate generating signal generator output.
*/

s_status = rspfg_InitiateGeneration (s_VI);

/*
  Start generating signal generator output.
*/

s_status = rspfg_SendChannelSoftwareTrigger (s_VI, "CH1");

/*
  Stop generation of output signal.
*/

s_status = rspfg_AbortGeneration (s_VI);

/*
  Configure channel one for external trigger input at XTII1.
*/

s_status = rspfg_ConfigureTriggerSource (s_VI, "CH1",
                                         RSPFG_VAL_TRIG_XTII1);

/*
  Initiate generating signal generator output.
*/

s_status = rspfg_InitiateGeneration (s_VI);
```



```
/*
  Configure channel one trigger delay.
*/

s_status = rspfg_ConfigureTriggerDelay (s_VI, "CH1", 1.0);

/*
  Initiate generating signal generator output.
*/

s_status = rspfg_InitiateGeneration (s_VI);

/*
  Wait for an external trigger input at front connector XT11.
*/

/*
  Stop generation of output signal.
*/

s_status = rspfg_AbortGeneration (s_VI);
}
```

8 Self-Test

The TS-PFG function generator has a built-in self-test capability. The following tests are possible:

- LED Test:
- Power-on test
- TSVP self-test

8.1 LED Test:

When the device is switched on, all three LEDs are lit for about one second. This indicates that the 5 V supply is present and all LEDs are working, also that the power-on test was successful. The following statements can be made about the different LED statuses:

LED	Description
One LED does not light up	Hardware problem on the module LED faulty
No LED's light up	No +5V supply

Table 8-1 Statements about the LED Test



NOTE:

If diagnostics suggest a problem with the supply voltage, the LEDs for the associated rear I/O module, TS-PDC, must be inspected visually. If a supply voltage failure is confirmed, the TS-PDC module must be replaced.

8.2 Power-on test

The power-on test runs at the same time as the LED test. In this test, the result of the FPGA loading process is calculated (FPGA = Field Programmable Gate Array). The following statements can be made about the different statuses of the red and green LEDs:

LED	Description
Green LED on	all supply voltages present
green LED off	at least one supply voltage of the TS-PFG module or the rear I/O module TS-PDC is missing
red LED off	no errors were detected
red LED on	FPGA loading failed

Table 8-2 Statements about the power-on test



NOTE:

If diagnostics suggest a problem with the supply voltage, the LEDs for the associated rear I/O module, TS-PDC, must be inspected visually. If a supply voltage failure is confirmed, the TS-PDC module must be replaced.

8.3 TSVP Self-Test

The TSVP self-test runs an in-depth test on the module and generates a detailed log. This is done with the “Self-Test Support Library”.

The TS-PSAM module is used as a measurement unit of R&S modules in the TSVP. The correct operation of the modules is ensured by measurements on the analog bus.



NOTE:

You will find information about starting the self-test and on the sequence of necessary steps in the GTSL software description or the GTSL on-line help.

9 Interface Description

9.1 Interface description for TS-PFG

9.1.1 Connector X10 (Front Connector)

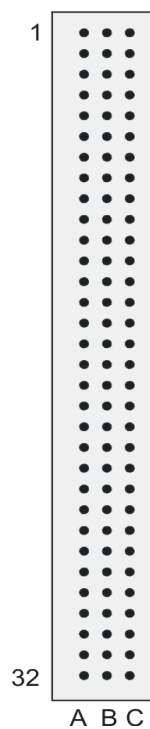


Figure 9-1 Connector X10 (mating side)

Pin	A	B	C
1	LABA1		LABA2
2	LABB1		LABB2
3	LABC1		LABC2
4	LABD1		LABD2
5			
6			
7			
8			
9			

Table 9-1 Pin assignment for connector X10



Pin	A	B	C
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28	GND	GND	GND
29	MO1	GND	MO2
30	XTI1	GND	XTI2
31	GND	GND	GND
32	GND	GND	CHA-GND

Table 9-1 Pin assignment for connector X10

* = Signal **CHA-GND** is connected to the front panel of the TS-PFG.
The front panel is capacitively coupled to GND.

9.1.2 Connector X20 (Extension Connector)

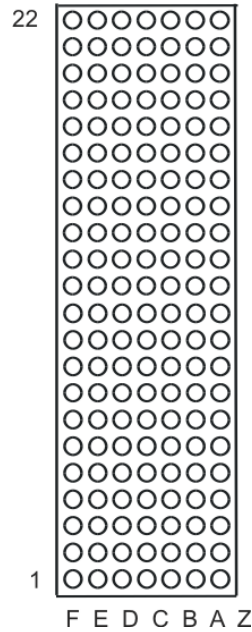


Figure 9-2 Connector X20 (mating side)

Pin	F	E	D	C	B	A	Z	
22	GND	GA0	GA1	GA2	GA3	GA4	GND	X20 C O N N E C T O R
21	GND	PXI_LBR3	PXI_LBR2	PXI_LBR1	GND	PXI_LBR0	GND	
20	GND	PXI_LBL1	GND	PXI_LBL0	AUX1	AUX2	GND	
19	GND	AUX1	AUX2	PXI_LBL3	GND	PXI_LBL2	GND	
18	GND	PXI_TRIG6	GND	PXI_TRIG5	PXI_TRIG4	PXI_TRIG3	GND	
17	GND	PXI_CLK10			GND	PXI_TRIG2	GND	
16	GND	PXI_TRIG7	GND		PXI_TRIG0	PXI_TRIG1	GND	
15	GND	+5V	+5V		GND	DCSYNC	GND	
14	NC						NC	
13	NC						NC	
12	NP	COM_CH1	+VCC3_1	+VCC2_CH1	-VCC1_CH1	+VCC1_CH1	NP	
11	NP						NP	
10	NC	COM_CH2	+VCC3_2	+VCC2_CH2	-VCC1_CH2	+VCC1_CH2	NC	
9	NC						NC	
8	NC						NC	
7	NC						NC	
6	NC						NC	
5	NC						NC	
4	NC						NC	
3	GND	RSA0	RRST#	+12V	GND	RSDO	GND	
2	GND	+12V	RSDI	RSA1	+5V	RSCLK	GND	
1	GND	+5V			GND	RCS#	GND	

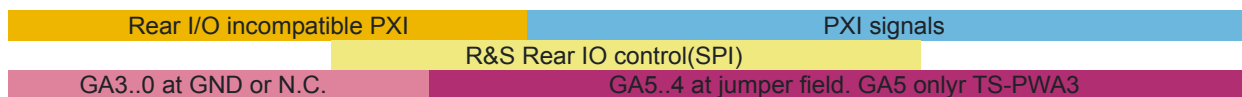


Table 9-2 Pin assignment for connector X20

9.1.3 Connector X30 (Analog Bus Connector)

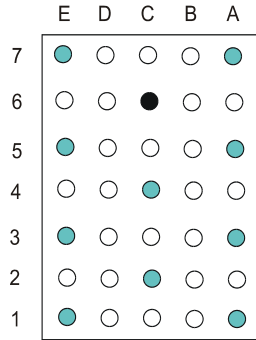


Figure 9-3 Connector X30 (mating side)

	E	D	C	B	A
7	IL2				IL1
6			GND		
5	ABA1				ABA1
4			ABB1		
3	ABC2				ABB2
2			ABA2		
1	ABD2				ABD1

Table 9-3 Pin assignment for connector X30

9.1.4 Connector X1 (cPCI Bus Connector)

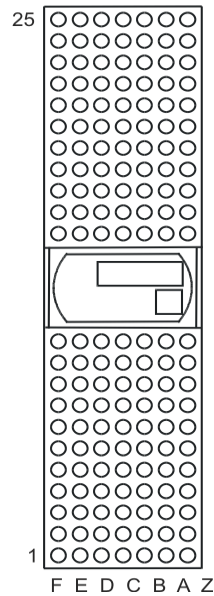


Figure 9-4 Connector X1 (mating side)

Pin	F	E	D	C	B	A	Z		
25	GND	5V	3.3V	ENUM#	REQ64#	5V	GND	X1 C O N N E C T O R	
24	GND	ACK64#	AD[0]	V(I/O)	5V	AD[1]	GND		
23	GND	AD[2]	5V	AD[3]	AD[4]	3.3V	GND		
22	GND	AD[5]	AD[6]	3.3V	GND	AD[7]	GND		
21	GND	C/BE[0]#	M66EN	AD[8]	AD[9]	3.3V	GND		
20	GND	AD[10]	AD[11]	V(I/O)	GND	AD[12]	GND		
19	GND	AD[13]	GND	AD[14]	AD[15]	3.3V	GND		
18	GND	C/BE[1]#	PAR	3.3V	GND	SERR#	GND		
17	GND	PERR#	GND	IPMB_SDA	IPMB_SCL	3.3V	GND		
16	GND	LOCK#	STOP#	V(I/O)	GND	DEVSEL#	GND		
15	GND	TRDY#	BD_SEL#	IRDY#	FRAME#	3.3V	GND		
12..14	Key Area								
11	GND	C/BE[2]#	GND	AD[16]	AD[17]	AD[18]	GND		
10	GND	AD[19]	AD[20]	3.3V	GND	AD[21]	GND		
9	GND	AD[22]	GND	AD[23]	IDSEL	C/BE[3]#	GND		
8	GND	AD[24]	AD[25]	V(I/O)	GND	AD[26]	GND		
7	GND	AD[27]	GND	AD[28]	AD[29]	AD[30]	GND		
6	GND	AD[31]	CLK	3.3V	GND	REQ#	GND		
5	GND	GNT#	GND	RST#	BSRSV	BSRSV	GND		
4	GND	INTS	INTP	V(I/O)	HEALTHY#	IPMB_PWR	GND		
3	GND	INTD#	5V	INTC#	INTB#	INTA#	GND		
2	GND	TDI	TDO	TMS	5V	TCK	GND		
1	GND	5V	+12V	TRST#	-12V	5V	GND		

Table 9-4 Pin assignment for connector X1

9.2 Interface description for TS-PDC

9.2.1 Connector X20 (Extension Connector)

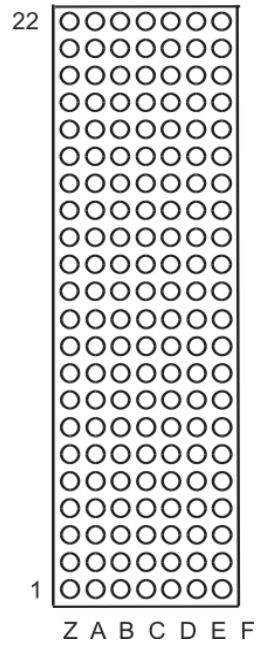


Figure 9-5 Connector X20 (TS-PDC mating side)



Pin	Z	A	B	C	D	E	F		
22	GND						GND	J20	
21	GND		GND or NC *3)				GND		
20	GND			+5V *1)	GND	+5V *1)	GND		
19	GND		GND	+5V *1)			GND		
18	GND				GND		GND		
17	GND		GND	+5V *2)	+5V *2)		GND		
16	GND			+5V *2)	GND		GND		
15	GND		GND	+5V *2)	+5V *1)		GND		
14	NC						NC		C O N N E C T O R
13	NC						NC		
12	NP	+15V_1	-15V_1	+5V_1	+3.3V_1	COM_1	NP		
11	NP						NP		
10	NC	+15V_2	-15V_2	+5V_2	+3.3V_2	COM_2	NC		
9	NC						NC		
8	NC	COM_1	COM_1	COM_1	COM_1	COM_1	NC		
7	NC						NC		
6	NC	COM_2	COM_2	COM_2	COM_2	COM_2	NC		
5	NC						NC		
4	NC						NC		
3	GND		GND		RRST#		GND		
2	GND	RSCLK			RSDI		GND		
1	GND	RCS#	GND			+5V *1)	GND		
Pin	Z	A	B	C	D	E	F		

- *1) TS-PDC V1.0 is supplied via these pins from +5V, for backplanes up to V3.x
- *2) TS-PDC V1.1 is supplied via these pins or pins from *1) , for backplanes V1.x to V4.x
- *3) TS-PDC V1.1 and V1.2: GND, for version V1.3: NC (Not Connected)

Table 9-5 Pin assignment for connector X20 (TS-PDC)



10 Specifications


NOTE:

In the event of any discrepancies between data in this manual and the technical data in the data sheet, the data sheet takes precedence.

10.1 Interface

Trigger interface:	cPCI interface to PICMG 2.0 Rev. 2.1
Front panel connectors:	96-way DIN strip to 41612
Space requirement:	1 slot in the front, 1 slot at rear (floating supply with TS-PDC)

10.2 Signal Generation

Analog channels:	2, differential, short-circuit proof, floating, cascadable, can be operated synchronously or asynchronously as 2 separate generators
Digital marker channels:	2, (TTL)
Data storage (RAM):	1 MSamples per channel
Signal forms:	DC Sine max. 1 MHz Square max. 1 MHz Mark/space ratio 1% ... 99% Triangular max. 1 MHz Sawtooth max. 1 MHz User-defined curve forms

10.3 Time Control

Modes:	DC mode, burst, continuous
Burst Mode	
• Scanning frequency:	DC, 1 S/s ... 25 MS/s
• Resolution:	40 ns min.
• Sequence linking:	64 per channel, max. 16384 cycles per sequence
Continuous Mode	
• Frequency:	1 Hz ... 1 MHz sine
• Resolution:	0.004% of the set value
• Accuracy:	Resolution \pm (resolution + reference clock accuracy)
Reference Clock:	PXI-Clock TSVP, 10 MHz, \pm (1.5 ppm + 1 ppm/year)

10.4 Output Levels

Amplitude	
• Ranges:	± 20 V, ± 10 V, ± 5 V, ± 1 V (40 Vpp, 20 Vpp, 10 Vpp, 2 Vpp)
• Resolution:	16 bit
• Accuracy:	see table

Amplitude			
Amplitude		Frequency 1 Hz ... 100 kHz	Frequency 10 Hz ... 1 MHz
Range	Resolution	Error Limits	Error Limits
20 V	0.6 mV	± 0.25 dB	± 0.5 dB
10 V	0.3 mV	± 0.25 dB	± 0.5 dB
1 V	0.03 mV	± 0.3 dB	± 0.5 dB

Offset	
• Range:	-20 V ... +20 V (offset + amplitude less than range limit)
• Resolution:	12 bit
• Accuracy:	see table



DC / Offset		
Range	Resolution	Error Limits
±20 V	10 mV	±(1% +100 mV)
±10 V	5 mV	±(1% +80 mV)
±1 V	0.5 mV	±(1% +20 mV)

Output current: 250 mA max. (50 mA square >500 kHz)

Output impedance: <2.5 Ω, typically 1.25 Ω

Coupling: DC

Output bandwidth

- with low-pass filter (3 dB): 3 MHz / 100 kHz / 3 kHz (selectable)

Output potential: 1 potential per channel, max. working voltage 125 V

Temperature range: 23 ±5°C

Temperature coefficient (for 5° ... 40°C)

- Amplitude: 0 ... -0.05% / °C
- Offset: 0 ... -0.4% / °C of final value

10.5 Synchronization

(per channel)

Trigger inputs: 1x local TTL trigger, 8x PXI trigger bus

Edge: positive / negative edge

Pattern: 9 bit, 3 states: High, Low, don't care

Delay: 40 ns ... 100 s

Trigger Outputs: 1x local TTL trigger (marker synchronous with analog signal) 8x PXI trigger bus (marker channels can be used as additional channels with digital signals)

10.6 Primary Connection

Front connector:	2x 8:1 multiplexer, 2-pole on local analog bus
R&S Analog bus access:	8x coupling relays to the analog bus
Max. switching voltage:	125 V / 125 V _{rms}
Max. switching current:	1.0 A / 1.0 A _{rms}
Max. power:	10 W / 10 VA
Insulation: (channel-to-channel, channel-to-GND)	125 V

10.7 General Data

Power consumption:	+5 V / 5.8 A +3.3 V / 0.2 A, 30 W max. incl. TS-PDC
EMC:	according to EMC Directive 89/336/EEC and Standard EN61326
Safety:	CE, EN61010 Part 1
Mechanical strength	
• Vibration test sinusoidal	
Sinus 5 Hz ... 55 Hz:	2 g, MIL-T-28800D, class 5
Sinus 55 Hz ... 150 Hz:	0.5 g, MIL-T-28800D, class 5
• Vibration test random	
10 Hz ... 300 Hz:	1.2 g
Shock test:	40 g, MIL-STD-810. Classes 3 and 5
Temperature load	
• Nominal temperature range:	+5 ... +40 °C
• Operating temperature range:	+0 ... +50 °C
• Storage temperature range:	-40 ... +70 °C
• Humidity:	+40°C, 95% RH
Dimensions in mm:	316 x 174 x 20



Weight:	0.50 kg max., 0.80 kg incl. TS-PDC
Calibration interval: (recommended)	1 year

10.8 Ordering Information

Function Generator TS-PFG (incl. TS-PDC)	1158.0052.02
Platform, TS-PCA3	1152.2518.02